<u>Amendments to the Claims</u>

1. (Currently Amended) A commercially mass-produced, integrated circuit comprising:

a solid substrate of one conductivity type;

~~at least one~~ <u>a</u> solid material pocket of a different conductivity type having a side surface and positioned on a selected top surface of said substrate ~~to thereby form~~<u>;</u>

a signal-translating, electronic rectifying barrier between said ~~at least one~~ solid material pocket and the selected top surface of said substrate; and

a solid state material region adjoining said <u>solid</u> substrate, said electronic rectifying barrier, and the side surface of said [at least one] solid material pocket;

~~wherein next to said electronic rectifying barrier~~ said solid state material region ~~has a lateral dimensional~~ <u>having a depth</u> accuracy of better than [a few hundred atomic layers] <u>0.13 microns; and</u>

<u>said solid state material region being continuously and perfectly bonded metallurgically to all said solid substrate, said solid material pocket, and said rectifying barrier, without thermally and electrically insulating voids and microcracks visible at 1,000 times magnification in interfacial bonding regions between the device components</u> .

2. Canceled.

3. (Currently Amended) A mass-produced integrated circuit as in claim 1 in which a lateral edge of at least one of said <u>solid</u> substrate, said solid material pocket, and said electronic rectifying barrier has a lateral dimensional accuracy of a few hundred atomic layers.

4. Canceled.

5. (Currently Amended) A mass-produced integrated circuit as in claim 1 in which a selected significant portion of a major surface of at least ~~a number~~ one of said ~~at least one~~ solid material pocket, [[the]] said selected top surface of said substrate, said solid state material region, and said electronic rectifying barrier gradually changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier;

said number being selected from the group consisting of one, two, and three.

6. (Currently Amended) A mass-produced integrated circuit as in claim 1 in which a [[major]] selected significant portion of at least one of said ~~at least one~~ solid material pocket, said selected top surface of said solid substrate, said solid state material region, and said electronic rectifying barrier montonically changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

7. Canceled.

8. (Currently amended) A mass-produced integrated circuit as in claim 1 in which at least a major surface of one of said electronic rectifying barrier and said ~~at least one~~ solid material pocket is curved.

9. Canceled.

10. (Currently Amended) A mass-produced integrated circuit as in claim 1 in which the side surface of said ~~at least one~~ solid material pocket is curved over a major portion thereof~~, and gradually decreases in radius of curvature with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier~~.

11. Canceled.

12. Canceled.

13. Canceled.

14. Canceled.

15. (Original) A mass-produced integrated circuit as in claim 1 in which at least one of top and bottom major surfaces of said electronic rectifying barrier is curved.

16. (Currently Amended) A mass-produced integrated circuit as in claim 1 in which a selected portion of said electronic rectifying barrier has a vertical thickness which gradually ~~decreases~~ increases with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier.

17. Canceled.

18. (Currently Amended) A mass-produced integrated circuit as in claim 1 in which said electronic rectifying barrier ~~region~~ is thin and has a laterally-extending dimension of less than one micron.

19. (Currently Amended) A mass-produced integrated circuit as in claim 1 in which:

said solid state material region consists essentially of a solid material selected from the group consisting of ~~a solid~~ oxide, glass, organics, semiconductor, metal, intermetallics, organics, semiconductor, a dielectrics material, and an electrically insulating solid ~~, and a gas~~;

said electronic rectifying barrier is selected from the group consisting of a PN junction, a heterojunction, a metal-oxide junction, and a Schottky barrier; and

said ~~at least one~~ solid material pocket is of a semiconductor material selected from the group consisting of Ge, Si, GaAs, GaP, InP, InSb, other III-V semiconductor compounds, other II-VI semiconductor compounds, and mixture thereof.

20. (Currently amended) A mass-produced, miniaturized semiconductor device comprising:

a first semiconductor material body having a first polarity;

a second semiconductor material body located generally vertically underneath said first semiconductor material body and [[has]] having a second polarity that is opposite the first polarity;

~~said first and second semiconductor material bodies adjoining to form at least one~~ a signal-translating, electronic rectifying barrier formed between said first and second semiconductor material bodies ~~therebetween~~; and

a third solid state material body having an electrical conductivity at least one order of magnitude different form those of said first and second semiconductor material bodies;

said third solid state material body contacting respective portions of each of said first and second semiconductor material bodies and said electronic rectifying barrier, and having two differentially surface-expanded sides that are not parallel to each other to form a terminal portion of no more than a micron in thickness in a selected direction; and

said thickness being accurate to within a few hundred atomic layers.

21. Canceled.

22. (Currently Amended) A semiconductor device as in claim 20 in which at least one of said first semiconductor material body, said second semiconductor material body, and [[third]] said third solid state material body ~~bodies~~ is of an intrinsic semiconductor material.

23. (Currently Amended) A semiconductor device as in claim 20 in which said third solid state material body has an as-formed metallurgically graded-seal continuity of a graded-seal type with respect to at least one of said first and second ~~solid body~~ semiconductor material bodies.

24. (Currently Amended) A semiconductor device as in claim 20 in which the terminal portion of said third solid state material body is vertically within less than a distance from a selected point inside said electronic rectifying barrier;

said distance being selected from the group consisting of one micron and 0.1 ~~micron~~ microns.

25. (Currently Amended) A semiconductor device as in claim 20 in which said third solid state material body has a geometry, position, and orientation relative to said first and second semiconductor material bodies, ~~and formative conditions~~ to allow adequate stress and strain ~~relief~~ modification on said electronic rectifying barrier thereby improving device performance.

26. (Currently Amended) A semiconductor device as in claim 25 in which said third solid state material body is favorably ~~compressed~~ stressed, and ~~having~~ has a blunt and rounded bottom of zero width so that lateral mismatch stresses at the bottom in the zero width direction is also zero, and

in which ~~said electronic rectifying barrier~~ the rounded bottom of said third solid state material body is located within a specified distance from a designated point inside said electronic rectifying barrier to achieve a beneficial proximity effect;

said specified distance being selected from the group consisting of one micron and 0.1 microns.

27. Canceled.

28. (Currently Amended) A semiconductor device as in claim 20 in which said third solid state material body is of an electrically insulating material selected from the group consisting of [[air,]] an oxide, a nitride, ~~another solid,~~ organics, semiconductor, metal, intermetallics, a dielectric material, other insulator, or a mixture thereof.

29. Canceled.

30. (Currently Amended) A semiconductor device as in claim 20 in which said third solid state material body has a designed, three-dimensionally controlled shape, size, and location[, and chemical composition] accurate to fractional microns.

31. (Currently amended) A semiconductor device as in claim 20 in which said third solid state material body has a rounded portion forming an inverted arch making the device more mechanically stable and reliable.

32. (Currently Amended) A semiconductor device as in claim 20 in which the terminal portion of said third solid state material body is less than 1 micron wide in a selected direction.

33. (Currently amended) A semiconductor device as in claim 20 in which said electronic rectifying barrier [[is]] has a curved major surface.

34. (Currently Amended) A semiconductor device as in claim 20 in which said third solid state material body has ~~two sides which generally conform to~~ a cylindrical surface.

35. Canceled.

36. (Currently Amended) A semiconductor device as in claim 20 in which ~~at least one of said third solid body and~~ said

electronic rectifying barrier is stressed to improve a performance of said semiconductor device.

37. Canceled.

38. (Currently Amended) A semiconductor device as in claim 20 in which:

said third solid state material body consists essentially of a material selected from the group consisting of a solid, an electrically insulating solid, oxide, glass, organics, semiconductor, metal, intermetallics, a dialectical material, and a mixture thereof ~~and a gas~~;

said ~~signal-translating,~~ electronic rectifying barrier is selected from the group consisting of a PN junction, PI junction, NI junction, metal-oxide, oxide-semiconductor, interfacial rectifying barrier, and heterojunction, and other optoelectromagnetically active signal-translating region, [[and]] a Schottky barrier; and a mixture thereof;

said first semiconductor material body is of a semiconductor material selected from the group consisting of Ge, Si, GaAs, GaP, InP, InSb, other III-V semiconductor compounds, other II-VI semiconductor compounds, and mixture thereof.

39. Canceled.

40. Canceled.

41. Canceled.

42. Canceled.

43. Canceled.

44. Canceled.

45. (Currently amended) An integrated circuit ~~A semiconductor device~~ as in claim [[39]] 1 in which said electronic rectifying barrier adjoins both said solid substrate and said solid state material region at a place where a periphery of said electronic rectifying barrier is differentially surface-expanded to passivate the adjoining rectifying barrier and to reduce noise, instability, leakage current, electrical shorts, and failure due to low breakdown voltage ~~; said differential surface-expansion having an equivalent bevel angle of less than 2.56 degrees~~.

46. (Currently Amended) An integrated circuit ~~A semiconductor device~~ as in claim [[39]] 1 in which said solid state material region is a vertically elongated region of less than 1 micron in width or size with an accuracy of less than ~~a few hundred atomic layers~~ 0.13 microns, and having a bottom of a shape selected from the group consisting of flat, rounded, cylindrical, hemispherical, and conical or V-shaped.

47. (Currently Amended) An integrated circuit ~~A semiconductor device~~ as in claim [[39]] 1 including means for circulating a rapidly moving cooling fluid in a microscopic vicinity of said signal translating, electronic rectifying barrier to achieve surface cooling of said electronic rectifying barrier.

48. (Currently Amended) An integrated circuit ~~A semiconductor device~~ as in claim [[39]] 1 in which said electronic rectifying barrier has a lateral edge, and at least one of said ~~semiconductor~~ solid material pocket, said rectifying barrier, and said solid state material region has a portion thereof which gradually and continuously changes its vertical thickness with closeness to said lateral edge of said electronic rectifying barrier.

49. (Currently Amended) An integrated circuit ~~A semiconductor device~~ as in claim [[30]] 1 in which at least one of said ~~semiconductor~~ solid material pocket, said rectifying barrier, and said solid state material region has a selected portion thereof which gradually and ~~continuously decreases~~ montonically changes its vertical thickness with closeness to said lateral edge of said electronic rectifying barrier.

50. (Currently Amended) An integrated circuit ~~A semiconductor device~~ as in claim [[39]] 1 in which a selected portion of at least one of a major surface of said ~~semiconductor~~ solid material pocket, said electronic rectifying barrier, and said solid state material region is curved.

51. Canceled.

52. (Currently Amended) An integrated circuit ~~A semiconductor device~~ as in claim [[39]] 1 in which said solid state material region is an elongated deep and narrow, solid state material region; and including:

a second elongated deep and narrow, solid state material region ~~differing from said semiconductor material pocket in electrical conductivity in a way selected from the group consisting of significantly and by over one order of magnitude~~ microscopically close to said elongated deep and narrow, solid state material region;

each of said elongated, deep and narrow, solid state material region and said second elongated deep and narrow, solid state material region being within a micron of both said solid substrate and said electronic rectifying barrier;

said second elongated, solid state material region also having a second submicron width or size at a second terminal portion thereof where it is closest to said electronic rectifying barrier;

~~at a second selected longitudinal distance of no more than a few microns from said second terminal portion, a ratio of said~~

~~second selected longitudinal distance to said second submicron width or size exceeding 3;~~ and

both said elongated, solid state material region and said second elongated, solid state material region having aspect ratios exceeding 3, being oriented normally of a common major bottom surface of said solid substrate, and extending downward from a common top surface of said ~~semiconductor~~ solid material pocket whereby said elongated, solid state material region and said second elongated, solid state material region are parallel to each other.

53. (Currently Amended) A semiconductor device as in claim [[39]] 52 in which said elongated, solid state material region and said second elongated, solid state material region have different lengths so that these two solid state material regions reach different depths inside said [~~semiconductor material pocket~~] solid substrate.

54. (Currently Amended) A semiconductor device as in claim [[39]] 52 in which said elongated, solid state material region and said second elongated, solid state material region ~~is more electrically conductive than~~ differ in electrical conductivity by at least one order of magnitude from that of the material of said semiconductor material pocket.

55. Canceled.

56. (Currently Amended) An integrated circuit ~~A semiconductor device~~ as in claim [[39]] 1 in which:

material of said ~~semiconductor~~ solid material pocket [[is]] and said solid state material region are solids which are 100% dense, substantially chemically pure and uniform, and non-contaminating, and impervious to contaminating gases;

said solid state material region is ~~favorably compressed~~ stressed to favorably affect a device performance, and has a ~~blunt and~~ rounded bottom of zero width so that lateral mismatch

stresses at the bottom in the zero width direction is also zero, [[and]]

said electronic rectifying barrier is located within a specified distance, with a fractional micron accuracy, from a designated point inside said electronic rectifying barrier to achieve a beneficial proximity effect; and

said specified distance being selected from the group consisting of one micron and 0.1 microns.

57. (New) A mass-produced, low-cost miniaturized solid state device comprising:

a first solid state material of a first conductivity type, a second solid state material of a second conductivity type positioned under the first solid state material, the first and second solid state materials having respective adjoining portions;

a signal-translating, rectifying barrier region lying between the respective adjoining portions; and

a device material region starting at least in the first solid state material and extending toward the rectifying barrier region to form a bottom which is within a micron of a selected point inside the rectifying barrier region;

a major portion of a top surface area of device chip being occupied by device circuit elements themselves thereby achieving hitherto impossible, device miniaturization.

58. (New) A mass-produced, solid state device as in claim 57 in which the rectifying barrier region is selected form the group consisting of PN junction, metal-semiconductor or Schottky barriers, heterojunction, metal-oxide, other electrically rectifying barriers, and a mixture thereof;

at least one of the first and second solid state materials is selected from the group consisting of Si, Ge, GaAs, GaP, InP, InSb, intrinsic semiconductor, III-V semiconducting compound, II-VI semiconducting compound, and a mixture thereof;

the device material region penetrates through the rectifying barrier region to reach the second solid state material and, in combination with the rectifying barrier region; electrically isolates device components from one another; and

a bottom of the device material region is less than 0.1 microns and close to zero microns below the rectifying barrier region.

59. (New) A mass-produced, solid state device as in claim 57 in which the device material region has a bottom which is closer to zero microns than 0.1 microns below the rectifying barrier region.

60. (New) A mass-produced, solid state device as in claim 57 in which the device material region is an elongated device material region; is accurate to less than a micron in a dimension selected from the group consisting of shape, size, depth, and chemical composition profiling; and consists essentially of a device material selected from the group consisting essentially of air, a gas, oxide, nitride, glass, organics, semiconductor, metal, intermetallics, dialectical material, other electrically insulating material, and a mixture thereof.

61. (New) A mass-produced, solid state device as in claim 60 in which a bottom of the elongated device material region is close to zero microns below the rectifying barrier region .

62. (New) A mass-produced, solid state device as in claim 60 in which the elongated, device material region has an intentionally designed and produced rounded bottom having a curved peripheral surface thereat;

the rectifying barrier region adjoining the rounded bottom of the elongated device material region and having a matching curved peripheral surface thereon thereby passivating and differentially expanding greatly the curved peripheral surface of the rectifying barrier region for protection against Type I contaminants, for eliminating wasteful central flat portions at bottoms of similar device material regions in prior art devices, for reducing mismatch thermal stresses leading to electrical device failures, for minimizing electrical field gradient across a surface passivated and expanded, rectifying barrier region, and for improving mechanical and electrical device yields and reliabilities.

63. (New) A mass-produced, solid state device as in claim 57 in which only a minor portion of a top surface area of device chip is not occupied by device circuit elements themselves;

said device circuit elements having no centrally large and flat bottoms as in oxidized isolation bottoms of Peltzer and Murphy devices, thereby achieving radically improved device miniaturization.

64. (New) A mass-produced, solid state device as in claim 57 in which the first solid state material is purposely broken up into a plurality of smaller material patches so that mismatch stresses from varying coefficients of material thermal expansions are reduced in proportion to the smaller size of the broken material patches thereby improving device performance.

65. (New) A mass-produced, solid state device as in claim 57 in which the device material region is an elongated, cylindrical device material groove having both an aspect ratio of over 3 to 5 and a cylindrical radius of less than one micron, and

is oriented generally normally of a top surface of the second solid state material.

66. (New) A mass-produced, solid state device as in claim 65 in which the elongated, cylindrical device material groove is purposely tilted relative to atop surface of the second solid state material so that the device material groove is above a bottom plane of the rectifying barrier region at some places where the groove depth is less than zero (or $h<0$), substantially coincides with the same bottom plane of the rectifying barrier region at another place where the groove depth is zero (i.e., $h = 0$), but lies below the same bottom plane of the rectifying barrier region at other places where the growth depth is greater than zero (or $h>0$).

67. (New) A mass-produced, solid state device as in claim 65 in which the elongated, cylindrical device material groove has a cylindrical radius of less than one micron.

68. (New) A mass-produced, solid state device as in claim 65 including at least one additional, elongated, cylindrical device material groove oriented normally of a top surface of the second solid state material, and microscopically close to the other elongated, cylindrical device material groove;

both the two device material grooves having sizes of less than two microns and different lengths to thereby extend vertically downward from a common higher, vertical level to different depths into the second solid state material.

69. (New) A mass-produced, solid state device as in claim 65 in which a bottom of the elongated cylindrical device material groove is above the rectifying barrier region so as to have a groove depth of less than 0.1 microns but microscopically close to zero microns and designed specifically for at least one of thermal, magnetic, and electrical contacting or for optical

communication to the device, without actual physical exposure to ambient of the second solid state material.

70. (New) A mass-produced, solid state device as in claim 65 in which the elongated, cylindrical device material groove is real-time feed-back controlled to submicron accuracy in a depth to as close to zero microns below the rectifying barrier region as possible, yet still to have a meaningful device yield to be commercially viable because of the submicron depth accuracy.

71. (New) A mass-produced, solid state device as in claim 65 in which the elongated, cylindrical device material groove has a rounded bottom; and

the rectifying barrier region adjoins a rounded bottom of the device material groove at a curved peripheral surface thereof, thereby maximizing the peripheral surface expansion and minimizing electrical field gradient across the rectifying barrier region to improve device yield and manufacturability.

72. (New) A mass-produced, solid state device as in claim 57 in which the device material region is an elongated groove having a microscopically precise groove bottom surface suitable for introducing a precise amount and shape of a foreign matter through the newly formed, highly precise groove bottom surface, thereby achieving microscopically precise three-dimensional control as to shape, size, and position of a region of the foreign matter introduction into the device.

73. (New) A mass-produced, solid state device as in claim 57 in which the device material region is a vertical and electrically insulating, elongated device material groove; and

a lower end of the vertical, elongated groove has a centrally rounded bottom of substantially zero width in a direction parallel to a top major surface of the second solid state material whereby mismatch stresses in the direction arising from varying coefficients of thermal expansions of different

materials in the device are substantially zero in the direction thereby improving device yield, performance, and reliability.

74. (New) A mass-produced, solid state device as in claim 57 in which the rectifying barrier region has a curved peripheral surface to achieve enhanced device reliability; increase yield; decreased cost; improved junction surface passivation; increased packing density; increased switching speed; reduced noise, instability, leakage current and electrical shorts; improved breakdown voltage; controlled carriers generation, movement, and recombination at or near the junction region peripheral surface; and regulated optoelectromagnetic interaction of the rectifying barrier region with ambient or contacting material.